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EXAMINER	
PEREZ DAPLE, AARON C	
ART UNIT	**PAPER NUMBER**
2154	

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/742,264	CONE ET AL.	
	Examiner	Art Unit	
	Aaron C Perez-Daple	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Application is in response to Application filed 12/19/00.

2. Claims 1-20 are presented for examination.

3. This Action is non-Final.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claims 5 and 6** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, claim 5 recites the limitation "the packet processor unit" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

6. As a dependent claim, claim 6 suffers from the same deficiencies as claim 5.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 1, 2, and 16-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (US 6,385,672 B1) (hereinafter Wang) in view of Bechtolsheim et al. (US 6,343,072 B1) (hereinafter Bechtolsheim).

9. As for claim 1, Wang discloses an apparatus, comprising:

a state-machine-based network protocol unit disposed on an integrated circuit, the network protocol unit having state machines (interfaces 121 and 122, controller 125, Fig. 1) to control other units of the integrated circuit and to process a network protocol corresponding to data throughput through the integrated circuit (col. 4, lines 44-67); and

a storage unit (buffer 126) disposed on the integrated circuit and coupled to the network protocol unit, the storage unit responsive to the network protocol unit to store and to control direction of the data throughput through the integrated circuit (col. 4, lines 44-67).

Although the Examiner interprets that Wang teaches all the limitations of the claimed invention as detailed above, Wang does not explicitly disclose that the storage unit (buffer 126, Fig. 1) and the state machine (interfaces 121 and 122, controller 125, Fig. 1) are disposed on the same integrated circuit. Bechtolsheim teaches the advantages of combining control and storage capabilities on a single integrated circuit in order to save space and easily integrate with a networking system (col. 1, lines 28-52). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Wang by disposing the storage unit and the state machine on the same integrated circuit in order to save space and easily integrate with a networking system, as taught by Bechtolsheim above.

10. As for claim 2, Wang teaches the apparatus of claim 1 wherein the storage unit comprises:

a first buffer to temporarily store data throughput through the integrated circuit in a first direction (transmit buffer 123, Fig. 1);

a second buffer to temporarily store data throughput through the integrated circuit in a second direction different from the first direction (receive buffer 124, Fig. 1); and

a controller coupled to the first and second buffers and responsive to the state machines to determine which of the first or second buffers forward their respective stored data (controller 125, Fig. 1, col. 4, lines 44-67).

11. As for claim 16, Wang teaches a method, comprising:

using state machines disposed on an integrated circuit to process network protocol information associated with data receivable by the integrated circuit (Fig. 1; col. 4, lines 44-67);

determining a destination of the data using the state machines (col. 4, lines 44-67);

storing the data in a storage unit (buffer memory 126, Fig. 1) disposed on the integrated circuit and forwarding the stored data from the storage unit to the destination based on a command from the state machines (col. 4, lines 44-67).

12. As for claim 17, Wang teaches the method of claim 16, further comprising:

using the state machines to issue a command related to a request for data (col. 4, lines 44-67);

in response to the command, assembling a packet having header information and the requested data (col. 5, lines 1-17); and

transmitting the assembled packet to a network device that requested the data via a state-machine-based bus protocol controller (col. 4, line 44 – col. 5, line 17).

13. As for claim 18, Wang teaches the method of claim 16, further comprising programming the state machines using information stored externally to the integrated circuit and loaded on to the integrated circuit during power up (CPU 104, Fig. 1; col. 11, lines 24-26).

14. As for claim 19, Wang teaches the method of claim 17 wherein the state machines include:

a first state machine to control processing of the command related to the request for data (controller 125, Fig. 1; col. 4, lines 44-67); and

a second state machine to control assembly of the packet having the header information and the requested data (MAC interface 122, Fig. 1; col. 4, lines 44-67).

15. As for claim 20, Wang teaches the method of claim 16 wherein the state machines include:

a first state machine to interface the integrated circuit to a network device (considered inherent to controller 125, Fig. 1, because this is necessary for the transmission/reception of data between devices as detailed in col. 4, lines 44-67);

a second state machine to control reception of data sent from the network device to the integrated circuit (considered inherent to controller 125, Fig. 1, because this is necessary for the reception of data between devices as detailed in col. 4, lines 44-67); and

a third state machine to control transmission of data sent from the integrated circuit to the network device (considered inherent to controller 125, Fig. 1, because this is necessary for the transmission of data between devices as detailed in col. 4, lines 44-67).

16. **Claims 11-13 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Bechtolsheim and in further view of Davidson, Jr. et al. (US 5,550,957) (hereinafter Davidson).

17. As for claims 11 and 12, Wang discloses a system, comprising:

a network device (cpu 104, Fig. 1; col. 1, lines 18-23); and

an integrated circuit coupled *with the network device* to receive data transmitted between *the network* and the network device (NIC 120, Fig. 1), the integrated circuit including:

a state-machine-based packet processor unit having state-machines to control other units of the integrated circuit and to process a network protocol corresponding to data throughput through the integrated circuit (interfaces 121 and 122, controller 125, Fig. 1; col. 4, lines 44-67); and

a storage unit coupled to the packet processor unit and responsive to the packet processor unit to store and to control direction of the data throughput through the integrated circuit (buffer 126; col. 4, lines 44-67).

Although the Examiner interprets that Wang teaches all the limitations of the claimed invention as detailed above, Wang does not explicitly disclose that the storage unit (buffer 126, Fig. 1) and the state machine (interfaces 121 and 122, controller 125, Fig. 1) are disposed on the same integrated circuit. Bechtolsheim teaches the advantages of combining control and storage capabilities on a single integrated circuit in order to save space and easily integrate with a networking system (col. 1, lines 28-52). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Wang by disposing the

storage unit and the state machine on the same integrated circuit in order to save space and easily integrate with a networking system, as taught by Bechtolsheim above.

Furthermore, although obvious to one of ordinary skill in the art, Wang and Bechtolsheim do not specifically disclose transmitting and receiving data between the apparatus and a printer. Davidson teaches transmitting data on a network between host devices and a printer using a network interface (Fig. 1; col. 1, lines 12-51). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Wang and Bechtolsheim by transmitting and receiving data between the apparatus and a printer in order to share a printer over a network, as taught by Davidson (Fig. 1; col. 1, lines 12-51).

18. As for claim 13, Wang discloses the system of claim 11 wherein the storage unit comprises:

a first buffer to temporarily store data throughput through the integrated circuit in a first direction (transmit buffer 123, Fig. 1);

a second buffer to temporarily store data throughput through the integrated circuit in a second direction different from the first direction (receive buffer 124, Fig. 1); and

a controller coupled to the first and second buffers and responsive to the state machines to determine which of the first or second buffers forward their respective stored data (controller 125, Fig. 1, col. 4, lines 44-67).

19. As for claim 15, Wang discloses the system of claim 11 wherein the integrated circuit further comprises:

a packet assembler unit (MAC interface 122, Fig. 1) coupled to the packet processor unit to receive the commands related to data throughput within the integrated circuit, and being

responsive to the commands to retrieve data and to assemble a packet having header information and the retrieved data (col. 4, lines 44-67); and

a state-machine-based network device control component disposed on the integrated circuit and coupled to the packet processor unit, the network device control component having state machines to control transmission of packet data from the integrated circuit to a network device and reception of packet data from the network device to the integrated circuit (controller 125, Fig. 1; col. 4, lines 44-67).

20. **Claims 3-10 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Bechtolsheim and in further view of Hasan (US 6,044,416) (hereinafter Hasan).

21. As for claims 3 and 18, Wang teaches the apparatus of claim 1 and the method of claim 16, wherein the network protocol unit comprises part of a packet processor unit, the packet processor unit including a packet assembler interface through which to provide commands related to data throughput within the integrated circuit (interface between controller 125 and MAC interface 122, Fig. 1; col. 4, lines 44-67). Although arguably inherent to Wang, neither Wang nor Bechtolsheim specifically disclose an initialization unit to read information external to the integrated circuit and to use that information to program the state machines. Hasan teaches an initialization unit to read information external to the integrated circuit and to use that information to program the state machines in order to configure the state machines for use with different systems (col. 1, lines 39-58; Fig. 2). It would have been obvious to one of ordinary skill in the art to modify the teachings of Wang and Bechtolsheim by using an initialization unit to read information external to the integrated circuit and to use that

information to program the state machines in order to configure the state machines for use with different systems, as taught by Hasan above.

22. As for claim 4, Wang teaches the apparatus of claim 3, further comprising a packet assembler unit (MAC interface 122, Fig. 1) disposed on the integrated circuit and coupled to the packet assembler interface to receive the commands, the packet assembler unit responsive to the commands to retrieve data and to assemble a packet having header information and the retrieved data (col. 4, lines 44-67).

23. As for claim 5, Wang teaches the apparatus of claim 3, further comprising a state-machine-based network device control component disposed on the integrated circuit and coupled to the packet processor unit, the network device control component having state machines to control transmission of packet data from the integrated circuit to a network device and reception of packet data from the network device to the integrated circuit (controller 125, Fig. 1; col. 4, lines 44-67).

24. As for claim 6, Wang teaches the apparatus of claim 5 wherein the network device control component includes:

an arbiter to arbitrate for bus use associated with the transmission and the reception of the packet data (considered inherent to bus interface 121 and/or controller 125, Fig. 1, because an arbiter is required for interfacing with a bus, as understood by one of ordinary skill in the art; see col. 4, lines 44-67);

a first controller having logic to determine direction of the packet data (controller 125, Fig. 1; col. 4, lines 44-67); and

a second controller having logic to perform bus protocol associated with the packet data (bus interface 121, Fig. 1; col. 4, lines 44-67).

25. As for claim 7, Wang teaches the apparatus of claim 4, further comprising a port controller disposed on the integrated circuit and coupled to the packet processor unit, the port controller being capable to control transmission of data from the integrated circuit to an appliance and reception of data from the appliance to the integrated circuit (Fig. 1; col. 4, lines 44-67).

26. As for claim 8, Wang teaches the apparatus of claim 3, further comprising a controller disposed on the integrated circuit and coupled to the initialization unit (controller 125, Fig. 1), the controller having an interface (bus interface 121, Fig. 1) to receive the external information to program the state machines and to provide the received external information to the initialization unit (Fig. 1; col. 4, lines 44-67; col. 11, lines 24-26).

27. As for claim 9, Wang teaches the apparatus of claim 5 wherein the state machines of the network device control component include:

a first state machine to interface the network device control component to the network device (considered inherent to controller 125, Fig. 1, because this is necessary for the transmission/reception of data between devices as detailed in col. 4, lines 44-67);

a second state machine to control reception of packet data sent from the network device to the integrated circuit (considered inherent to controller 125, Fig. 1, because this is necessary for the reception of data as detailed in col. 4, lines 44-67); and

a third state machine to control transmission of packet data sent from the integrated circuit to the network device (considered inherent to controller 125 because this is necessary for the transmission of data between devices as detailed in col. 4, lines 44-67).

28. As for claim 10, Wang teaches the apparatus of claim 4 wherein the state machines include:

a first state machine associated with the packet processor unit to control processing of the data throughput through the integrated circuit (controller 125, Fig. 1; col. 4, lines 44-67); and

a second state machine associated with the packet assembler unit to control assembly of the packet (considered inherent to MAC interface 122, Fig. 1, because this in required for sending MAC packets over the network; col. 4, lines 44-67).

29. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Bechtolsheim and Davidson as applied to claim 11 above and in further view of Hasan. Claim 14 is subject to the same limitations as claims 3, 11 and 18 and is therefore rejected on the same grounds as claims 3, 11 and 18 above.

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

US 6,731,644 B1, note Fig. 1;

US 6,700,677 B1, note printer interface;

US 6,415,341 B1, note Fig. 4;

US 6,317,427 B1, note abstract;

US 6,256,687 B1, note Fig. 4;

US 6,128,673, note abstract;

US 5,875,415, note abstract;

US 5,434,872, note dedicated transmit buffer.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron C Perez-Daple whose telephone number is (703) 305-4897. The examiner can normally be reached on 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (703) 305-8498. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

9/27/04

Aaron Perez-Daple